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22879 7590 08/16/2010 HEWLETT-PACKARD COMPANY Intellectual Property Administration 3404 E. Harmony Road Mail Stop 35 FORT COLLINS, CO 80528			EXAMINER TSAL SIENG JEN	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LEITH JOHNSON

Appeal 2009-002162
Application 10/017,371¹
Technology Center 2100

Before JOSEPH L. DIXON, JAY P. LUCAS, and STEPHEN C. SIU,
Administrative Patent Judges.

LUCAS, *Administrative Patent Judge.*

DECISION ON APPEAL²

¹ Application filed December 7, 2001. The real party in interest is Hewlett-Packard Development Company.

² The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the “MAIL DATE” (paper delivery mode) or the “NOTIFICATION DATE” (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellant appeals from a final rejection of claims 1 to 5, 8 to 11, 14 to 21, 28, and 29 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b). Claims 6, 7, 12, 13, 22 to 27, 30, and 31 are cancelled.

We affirm the rejection.

Appellant's invention relates to a method for efficient memory management that involves translating a physical resource identifier into a machine resource identifier (Title and Spec. 9, middle). According to Appellant's lexicography, the claimed "physical resource identifier" and "machine resource identifier" (claim 1) correspond with a virtual memory address and a physical or hardware memory address, respectively, in the conventional art of computer memory. (See Spec. 16, middle.) In the words of Appellant:

[A] translation mechanism is provided for use in a partitionable server. The translation mechanism is logically interposed between the server's hardware memory resources and processes (such as operating systems and user processes) executing in partitions of the server. . . .

The translation mechanism maintains mappings between the partitions' physical address spaces and a "machine" address space that maps to the real (hardware) memory of the server.

(Spec. 12, top to middle).

Claim 1:

1. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, a method for creating a physical resource identifier space in a partition of the partitionable computer system, the method comprising steps of:

(A) establishing a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers, wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero, and wherein the mapping defines a non-monotonic function; and

(B) providing, to an operating system executing in the partition, an interface for the operating system to access the at least some of the plurality of machine resources using the plurality of physical resource identifiers.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Vishin

US 5,860,146

Jan. 12, 1999

REJECTION

The Examiner rejects the claims as follows:

Claims 1 to 5, 8 to 11, 14 to 21, 28, and 29 stand rejected under 35 U.S.C. § 102(b) for being anticipated by Vishin.

Appellant contends that Vishin does not anticipate the claimed subject matter for failure of the references to teach the limitation “providing ... an interface for the operating system to access the ... machine resources using the ... physical resource identifiers,” as required by claim 1 (App. Br. 14, middle). The Examiner contends that each of the claims is properly rejected (Ans. 13, middle).

We have only considered those arguments that Appellant actually raised in the Briefs. Arguments that Appellant could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUES

The issues involve whether Appellant has shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 102(b). The issues specifically turn on whether Vishin teaches Appellant’s claimed “interface” of claim 1 and whether the “operating system” itself must “access the ... machine resources using the ... physical resource identifiers” (claim 1).

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

Disclosure

1. Appellant has invented a method and apparatus for memory management that involves mapping between physical resource identifiers and machine resource identifiers. (*See* claims 1 and 8.) The method includes providing an interface for an operating system to access machine

resources using physical resource identifiers. (*See* claim 1.) The Specification discloses that Appellant’s “physical address space” maps only indirectly to hardware memory locations (Spec. 16, middle), whereas “machine addresses” refer to actual (hardware) memory resources (*id.*).

Vishin

2. The Vishin reference teaches translating virtual addresses into physical addresses (Abstract). The method includes providing application programs for an operating system to access the physical address spaces using the virtual addresses (col. 8, ll. 28-32).

PRINCIPLE OF LAW

Appellant has the burden on appeal to the Board to demonstrate error in the Examiner’s position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

ANALYSIS

Arguments with respect to the rejection of claims 1 to 5, 8 to 11, 14 to 21, 28, and 29 under 35 U.S.C. § 102(b)

The Examiner finds that connections between the operating system, the memory controller, and the remote translation lookaside buffer (RTLb) are the same as Appellant’s claimed “interface.” (*See* Ans. 10, top to middle.)

In reply, Appellant argues that the Vishin reference fails to meet the claim limitation “providing ... an interface for the operating system to

access the at least some of the plurality of machine resources using the plurality of physical resource identifiers,” because Vishin does not teach that “the operating system itself accesses machine resources ... using physical resource identifiers.” (App. Br. 14, middle).

We disagree with Appellant’s conclusion. We find that Appellant has invented a method and apparatus for memory management that involves mapping between physical resource identifiers and machine resource identifiers (FF#1). The method includes providing an interface for an operating system to access machine resources using the physical resource identifiers (*id.*). The Specification discloses that Appellant’s “physical address space” maps only indirectly to hardware memory locations, whereas “machine addresses” refer to actual (hardware) memory resources (*id.*). In comparison, we find that the Vishin reference teaches translating virtual addresses into physical addresses (FF#2). The method includes providing application programs for the operating system to access physical address spaces using the virtual addresses (*id.*).

We find that Appellant’s argument is not commensurate with the scope of claim 1’s language. Claim 1 does not require that “the operating system itself accesses machine resources,” as Appellant argues (App. Br. 14, middle). Rather, claim 1 requires an “interface ... to access the ... machine resources using the ... physical resource identifiers.” Although we import no limitation from the Specification (*see In re Van Geuns*, 988 F.2d at 1184), we examined the Specification closely for any indication that “the operating system itself accesses machine resources,” as Appellant argues (App. Br. 14, middle). We turn to the Specification, which discloses that a process executing “within” an operating system is properly interpreted as

“the operating system provides an environment in which the process may execute.” (Spec. 15, top). We thus read the claimed “interface” as “access[ing] machine resources ... using ... the physical resource identifiers” in the environment of the claimed “operating system.” That is, Appellant’s claim limitation is no different from Vishin’s teachings of remote memory mapping procedures provided by the operating system and available for use by application programs. (*See* FF#2.) Accordingly, we find no error.

As noted above, the Examiner finds that the claimed “interface” is the same as Vishin’s connections. (*See supra.*)

However, Appellant contends that Vishin does not teach any interface that is provided to the operating system for the operating system to access the plurality of machine resources (App. Br. 14, bottom).

We already answered Appellant’s argument, supplementing the Examiner’s response with our finding that Vishin’s application programs operate the same as “an interface,” as claimed (FF#1 and FF#2). Accordingly, we find no error.

Appellant further argues: “[Vishin’s] application programs, [and] not its operating system, access memory locations using virtual addresses, which are translated into physical addresses.” (App. Br. 15, top).

We previously addressed the above-stated argument. (*See supra.*) Accordingly, we find no error.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1 to 5, 8 to 11, 14 to 21, 28, and 29.

DECISION

We affirm the Examiner's rejection of claims 1 to 5, 8 to 11, 14 to 21, 28, and 29.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

peb

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